[Chapter 7]:- Universal Gates and physics of Integrated Circuits

Definition of Gates:

A digital circuit having one or more input signals but only one output signal is called a gate. There are two types of gates.

a. Basic [Fundamental] Gates: The gates which can be combined to produce other gates are called basic gates. There are three types of gate they are; OR, AND and NOT.
b. Derived [Compound] Gates: The gate which are derived by combining different basic gates are known as derived gates. There are five types of gate they are; NOR, NAND, X-OR and X-NOR.

❖ NAND and NOR gates are universal gates as all other gates can be designed using only either appropriate number of NAND and NOR gates.

Definition of Logic Gates:

A logic gate is an electronic circuit which makes logic decisions. It has one output and one or more inputs. The output signal appears only for certain combinations of input signals. Logic gates are the basic building blocks of the digital system. The voltage level at the input and output of these gates can have only two states, either high or low. The possible values of the inputs and output of these gates are 1 or 0.

Truth Table:

A truth table is a tabular representation of all the combinations of values for inputs and their corresponding outputs. It is a mathematical table that shows all possible outcomes that would occur from all possible scenarios that are considered factual, hence the name. Truth tables are usually used for logic problems as in Boolean algebra and electronic circuits.

Boolean Algebra:

Boolean algebra is the mathematics we use to analyze digital gates and circuits. We can use these "Laws of Boolean" to both reduce and simplify a complex Boolean expression in an attempt to reduce the number of logic gates required. Boolean algebra is therefore a system of mathematics based on logic that has its own set of rules or laws which are used to define and reduce Boolean expressions.

The variables used in Boolean Algebra only have one of two possible values, a logic "0" and a logic "1" but an expression can have an infinite number of variables all labelled individually to represent inputs to the expression.

De-Morgans Theorem

- The complement of a sum equals to the product of complements i.e. $\overline{A + B} = \bar{A}\bar{B}$
- The complement of the product equals to sum of the complements. $\overline{AB} = \bar{A} + \bar{B}$

This theorem is wrathful to simplify the complicated logical expression into simpler form.The above theorem can be proved truth table. For the truth table we use binary number system i.e. both A & B can have value either 0 or 1.

A	B	A+B	AB	$\bar{A}$	$\bar{B}$	$\overline{A+B}$	$\overline{AB}$	$\bar{A}+\bar{B}$	$\bar{A}\bar{B}$
0	0	0	0	1	1	1	1	1	1
0	1	1	0	1	0	0	1	1	0
1	0	1	0	0	1	0	1	1	0
1	1	1	1	0	0	0	0	0	0

Description of the Laws of Boolean Algebra:

i. Commutative Law – The order of application of two separate terms is not important.

a. $A \times B = B \times A$ The order in which two variables are AND'ed makes no difference.
b. $A + B = B + A$ The order in which two variables are OR'ed makes no difference.

ii. Distributive Law – This law permits the multiplying or factoring out of an expression.

- $A(B + C) = A \times B + A \times C$ (OR Distributive Law)
- $A + (B \times C) = (A + B) \times (A + C)$ (AND Distributive Law)

iii. Associative Law – This law allows the removal of brackets from an expression and regrouping of the variables.

a. $A + (B + C) = (A + B) + C = A + B + C$ (OR Associate Law)
b. $A(B \times C) = (A \times B)C = A \times B \times C$ (AND Associate Law)

iv. Absorptive Law – This law enables a reduction in a complicated expression to a simpler one by absorbing like terms.

a. $A + (A \times B) = A$ (OR Absorption Law)
b. $A(A + B) = A$ (AND Absorption Law)

v. Demorgan's Law:
$\overline{A + B} = \bar{A}\bar{B}$
$\overline{AB} = \bar{A} + \bar{B}$

In this chapter, we will consider the OR,AND,NOT,NOR,NAND exclusive OR (X-OR) and exclusive NOR (X-NOR).

1. OR Gate (IC 7432):

The OR gate is a digital logic gate that implements logical disjunction. An OR gate has two or more input signals but only one output signal. It is called an OR gate because the output voltage is high if any or all of the input voltages are high. The Boolean equation is, Y=A+B. The truth table and logic symbol of the OR gate with all possible inputs and corresponding output is as follows.

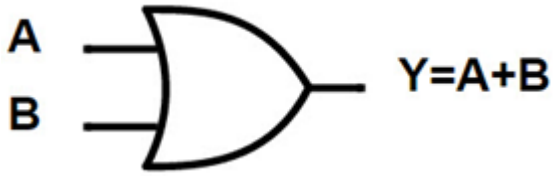


Fig: Logic symbol of OR Gate

Fig: Truth Table of OR Gate

Inputs		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Fig: Truth Table of Three inputs OR Gate

INPUTS			OUTPUT
A	B	C	Y=A+B+C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

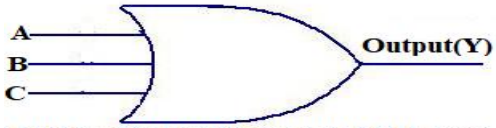


Fig: Symbol of Three input OR Gate

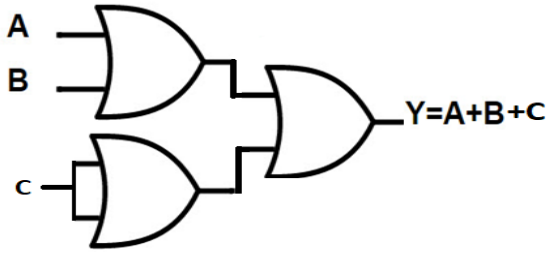


Fig: 3 input OR gate

OR Gate Using Diode: [Circuit Operation of OR Gate Using Diode]:

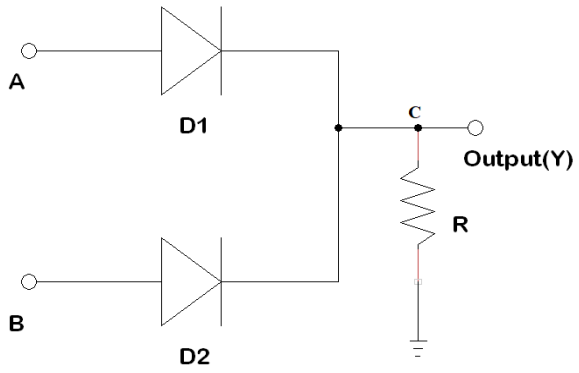


Fig: OR Gate using Diodes

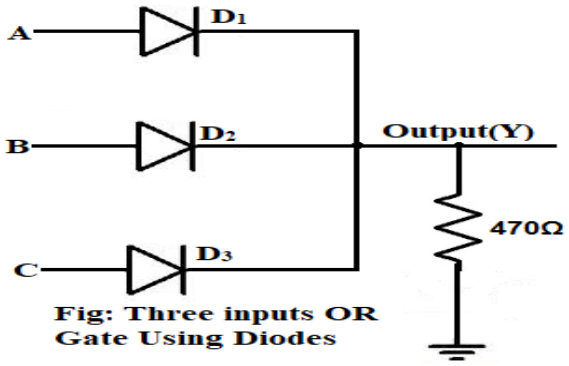


Fig: Three inputs OR Gate Using Diodes

- When A=0 and B=0 [both A and B are GND], both the diodes do not conduct (reverse biased) and no voltage develops across R. Therefore the voltage at C is zero with respect to earth. Hence the output Y is 0.
- When A = 0 and B = 1 (i.e., connected to positive terminal), the diode D_2 conducts (forward biased) but D_1 doesn't conduct (reverse biased). Since D_2 is ideal, no voltage drop takes place across D_2 and a full voltage drop of 5V takes place across R, at C, +5V with respect to GND. Therefore Y is 1.
- When A = 1 and B = 0, D_1 conducts but D_2 does not. For the same reason as stated above the output Y is 1.
- When A = 1 and B = 1, both diodes conducts since the diodes are ideal and connected in parallel, the voltage drop across R cannot exceed 5V, with C at +5V with respect to earth. Hence the output Y will be 1.

2. AND Gate [IC 7408]

The **AND gate** is a basic digital logic gate that implements logical conjunction. An AND gate has two or more input signals but only one output signal. It is called an AND gate because the output voltage is high if all of the input voltages are high. The Boolean equation is, Y=AB. The truth table and logic symbol of the AND gate with all possible inputs and corresponding output is as follows.

Fig: Logic symbol of AND Gate

Truth Table of AND Gate

Input	Input	Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

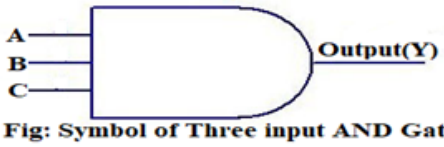


Fig: Symbol of Three input AND Gate

Truth Table of AND Gate

INPUTS			OUTPUT
A	B	C	Y=A.B.C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Truth Table of 3 Inputs AND Gate

AND Gate Using Diode: [Circuit Operation of AND Gate Using Diode]:

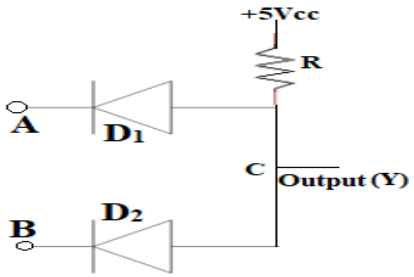


Fig: Circuit diagram of AND gate using diode

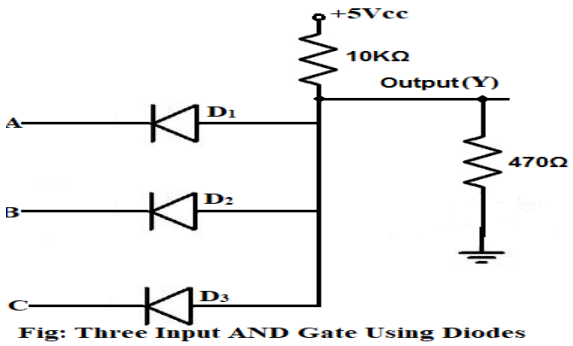


Fig: Three Input AND Gate Using Diodes

Working:

- When A = 0 and B = 0 both diode D_1 and D_2 get forward biased and hence conduct. The diodes being ideal, no voltage drop takes place across either diode. Therefore potential difference of 5V takes place across R, with C at zero potential with respect to GND. Thus the output Y is 0.
- When A = 0, B = 1, diode D_1 conducts diode D_2 doesn't conduct. Since D_1 is ideal, no voltage drop occurs it. Therefore voltage drop of 5V takes place across R and C at zero with respect to GND. The output is 0.
- When A = 1, B = 0 for same reason, output is 0.
- When A = 1, B = 1 none of diodes conduct and so no current flows through R. The potential at C is +5V with respect to GND. Hence output Y is 1.

3. NOT Gate [IC 7404]

The gate which complements the input is known as NOT gate. It is a gate with only one input and one output. If low input is given then is produces high output and vice-versa. It is also known as inverter as it inverts the input. Boolean expression for a Not gate is, $Y = \bar{A}$. The truth table and logic symbol of the NOT gate with all possible inputs and corresponding output are as follows.

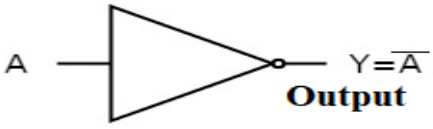


Fig: Logic symbol of NOT Gate

Input (A)	Output(Y)
1	0
0	1

Fig: Truth Table of OR Gate

Circuit operation of NOT Gate using Transistor Transistor Logic [TTL]:

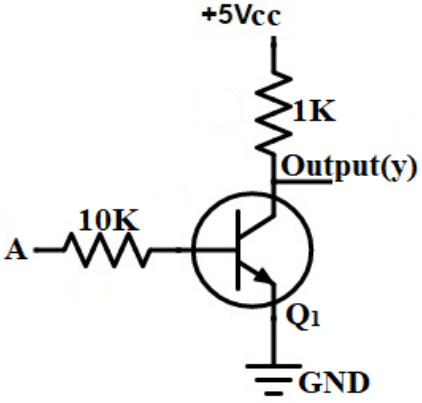


Fig: Circuit diagram of NOT gate using TTL

Working:

- When A=0,
  Base input of Q_1 is low, Q_1 is cutoff so that supply is blocked by Q_1 all Vcc current and voltage goes to output and hence it remains as output high [1]
- When A=1,
  Base input of Q_1 is high, Q_1 is saturated so that all Vcc current and voltage goes to GND and hence it remains as output low [0].

4. NOR Gate [IC7402]

A NOR gate has two or more input signals but only one output signal. It is called a NOR gate because the NOR gate is a combination of OR gate followed by an inverter or NOT gate. Its output is high if both inputs are low. Otherwise, the output is low. A NOR gate is just the reverse of OR gate. It's Boolean equation is $\mathbf{Y = \overline{A + B}}$ The truth table and logic symbol of the NOR gate with all possible inputs and corresponding output is as follows.

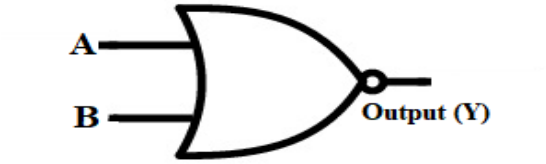


Fig: Logic Symbol of NOR Gate

Fig: Truth Table of NOR Gate

Input A	Input B	Output (Y)
0	0	1
1	0	0
0	1	0
1	1	0

NOR Gate Using Diode: [Circuit Operation of NOR Gate Using Diode]:

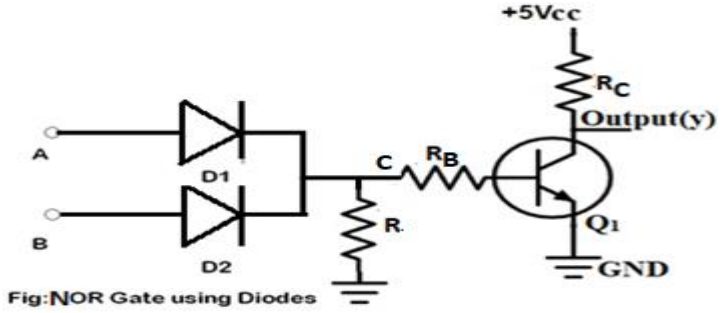


Fig:NOR Gate using Diodes

- **Working:** When A=0 and B=0 [both A and B are GND], both the diodes do not conduct (reverse biased) and no voltage develops across R. Therefore the voltage at C is zero with respect to earth. Hence Base input of Q_1 is low, Q_1 is cutoff so that supply is blocked by Q_1 all Vcc current and voltage goes to output and hence it remains as output high [1].
- When A = 0 and B = 1 (i.e., connected to positive terminal), the diode D_2 conducts (forward biased) but D_1 doesn't conduct (reverse biased). Since D_2 is ideal, no voltage drop takes place across D_2 and a full voltage drop of 5V takes place across R, at C, +5V with respect to GND. Hence base input of Q_1 is high, Q_1 is saturated so that all Vcc current and voltage goes to GND and hence it remains as output low [0].
- When A = 1 and B = 0, D_1 conducts but D_2 does not conduct. Since D_1 is ideal, no voltage drop takes place across D_1 and a full voltage drop of 5V takes place across R, at C, +5V with respect to GND. Hence base input of Q_1 is high, Q_1 is saturated so that all Vcc current and voltage goes to GND and hence it remains as output low [0].
- When A = 1 and B = 1, both diodes conducts since the diodes are ideal and connected in parallel, the voltage drop across R cannot exceed 5V, with C at +5V with respect to earth. Hence base input of Q_1 is high, Q_1 is saturated so that all Vcc current and voltage goes to GND and hence it remains as output low [0]

5. NAND Gate [IC7400]

A NAND gate has two or more input signals but only one output signal. It is called a NAND gate because the NAND gate is a combination of AND gate followed by an inverter or NOT gate. Its output is high if both or any one inputs are low. Otherwise, the output is low. A NAND gate is just the reverse of AND gate. It's Boolean equation is $\boldsymbol{Y = \overline{AB}}$ The truth table and logic symbol of the AND gate with all possible inputs and corresponding output is as follows.

Fig: Logic Symbol of NAND Gate

Inputs		output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig: Truth Table of NAND Gate

NAND Gate Using Diode: [Circuit Operation of NAND Gate Using Diode]:

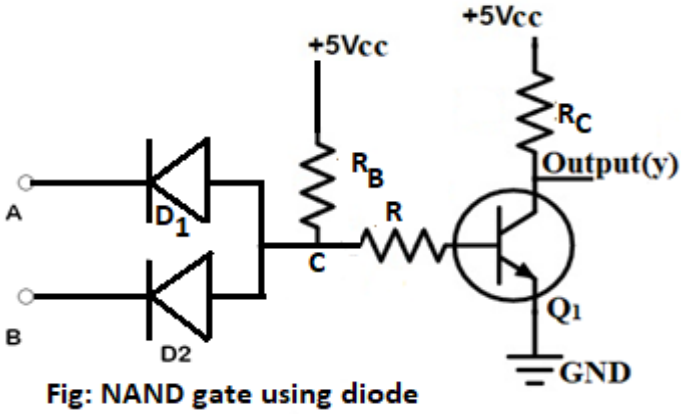


Fig: NAND gate using diode

- When A = 0 and B = 0 both diode D_1 and D_2 get forward biased and hence conduct. The diodes being ideal, no voltage drop takes place across either diode. Therefore potential difference of 5V takes place across R_B, with C at zero potential with respect to GND. Hence Base input of Q_1 is low, Q_1 is cutoff so that supply is blocked by Q_1 all Vcc current and voltage goes to output and hence it remains as output high [1].
- When A = 0, B = 1, diode D_1 conducts and diode D_2 doesn't conduct. Since D_1 is ideal, no voltage drop occurs it. Therefore voltage drop of 5V takes place across R_B, with C at zero with respect to GND. Hence Base input of Q_1 is low, Q_1 is cutoff so that supply is blocked by Q_1 all Vcc current and voltage goes to output and hence it remains as output high [1].
- When A = 1, B = 0 diode D_2 conducts and diode D_1 doesn't conduct. Since D_2 is ideal, no voltage drop occurs it. Therefore voltage drop of 5V takes place across R_B, with C at zero with respect to GND. Hence Base input of Q_1 is low, Q_1 is cutoff so that supply is blocked by Q_1 all Vcc current and voltage goes to output and hence it remains as output high [1].
- When A = 1, B = 1 none of diodes conduct and so no current flows through R. The potential at C is +5V with respect to GND. Hence voltage at R is 1. If base input of Q_1 is high, Q_1 is saturated so that all Vcc current and voltage goes to GND and hence it remains as output low [0].

Universal Gate

Universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families. In fact, an AND gate is typically implemented as a NAND gate followed by an inverter not the other way around. Likewise, an OR gate is typically implemented as a NOR gate followed by an inverter not the other way around.

NAND Gate is a Universal Gate:

To prove that any Boolean function can be implemented using only NAND gates, we will show that the OR, AND, NOT, NOR, X-OR & X-NOR operations can be performed using only these gates.

❖ **Implementing OR Gate Using only NAND Gates**

An OR gate can be replaced by NAND gates as shown in the figure (The OR gate is replaced by a NAND gate with all its inputs complemented by NAND gate inverters).

The alongside diagram is of an OR gate made from combinations of NAND gates, arranged in a proper manner.

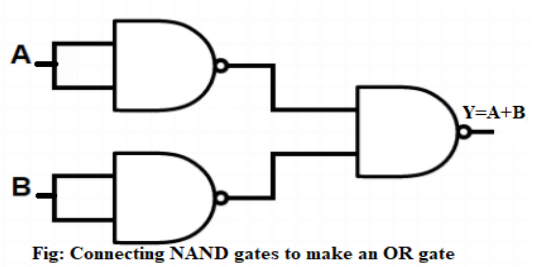


Fig: Connecting NAND gates to make an OR gate

❖ **Implementing AND Gate Using only NAND Gates**

An AND gate can be replaced by NAND gates as shown in the figure.

The alongside diagram is of an AND gate made from combinations of NAND gates, arranged in a proper manner.

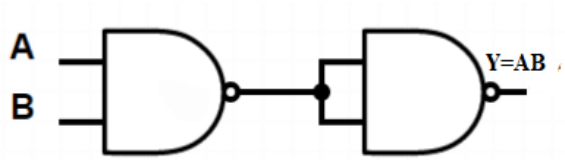


Fig: Connecting NAND gates to make an AND gate

❖ **Implementing NOT Gate Using only NAND Gates**

An NOT gate can be replaced by NAND gates as shown in the figure. The alongside diagram is of an NOT gate made from combinations of NAND gates, arranged in a proper manner. The truth table of an NOT gate is also given beside the diagram.

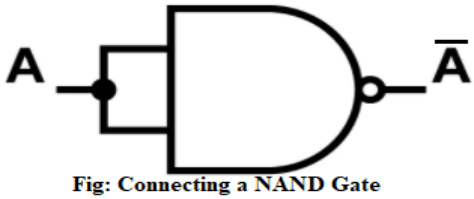


Fig: Connecting a NAND Gate to make a NOT Gate

❖ **Implementing NOR Gate Using only NAND Gates**

An NOR gate can be replaced by NAND gates as shown in the figure.

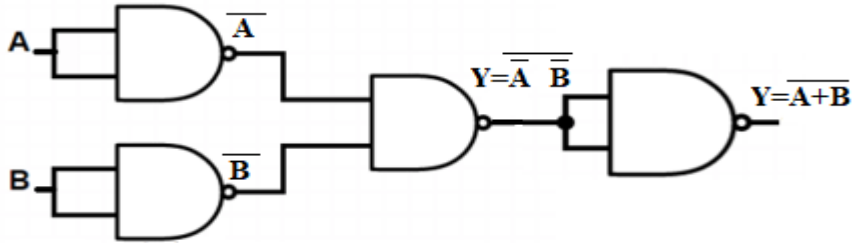


Fig: Connecting a NAND Gate to make a NOR Gate

❖ **Implementing X-OR Gate Using only NAND Gates**

An X-OR gate can be replaced by NAND gates as shown in the figure.

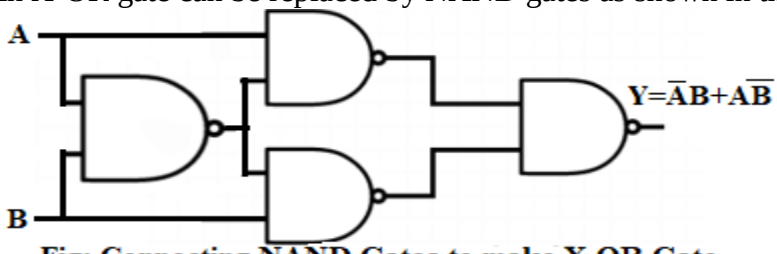


Fig: Connecting NAND Gates to make X-OR Gate

The above diagram is of an X-OR gate made from combinations of NAND gates, arranged in a proper manner. The truth table of an X-OR gate is also given beside the diagram.

❖ **Implementing X-NOR Gate Using only NAND Gates**

An X-NOR gate can be replaced by NAND gates as shown in the figure.

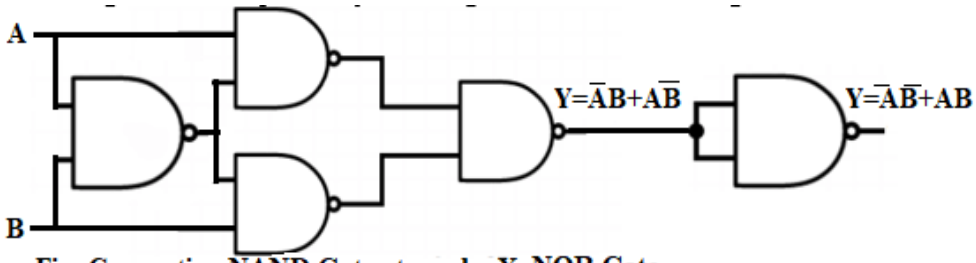


Fig: Connecting NAND Gates to make X- NOR Gate

The above diagram is of an X-NOR gate made from combinations of NAND gates, arranged in a proper manner. The truth table of an X-NOR gate is also given beside the diagram.

NOR Gate is a Universal Gate:

To prove that any Boolean function can be implemented using only NOR gates, we will show that the OR, AND, NOT, NAND, X-OR & X-NOR operations can be performed using only these gates.

- **Implementing OR Gate Using only NOR Gates**

  An OR gate can be replaced by NOR gates as shown in the figure.

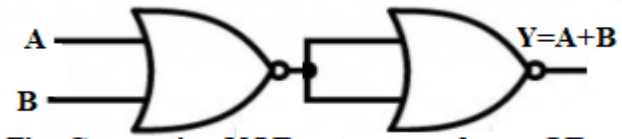


Fig: Connecting NOR gates to make an OR gate

The above diagram is of an OR gate made from combinations of NOR gates, arranged in a proper manner. The truth table of an OR gate is also given beside the diagram.

- **Implementing AND Gate Using only NOR Gates**

  An AND gate can be replaced by NOR gates as shown in the figure.

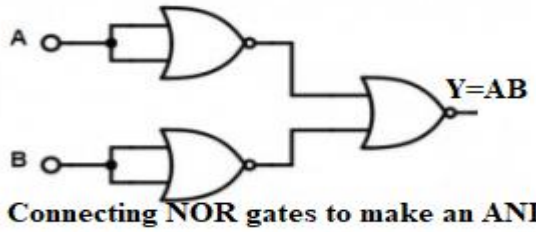


Fig: Connecting NOR gates to make an AND gate

The above diagram is of an AND gate made from combinations of NOR gates, arranged in a proper manner. The truth table of an AND gate is also given beside the diagram.

- **Implementing NOT Gate Using only NOR Gates**

  An OR gate can be replaced by NOR gates as shown in the figure.

Fig: Connecting NOR gates to make an NOT gate

The above diagram is of an NOT gate made from combinations of NOR gates, arranged in a proper manner. The truth table of an NOT gate is also given beside the diagram.

- **Implementing NAND Gate Using only NOR Gates**

  An NAND gate can be replaced by NOR gates as shown in the figure.

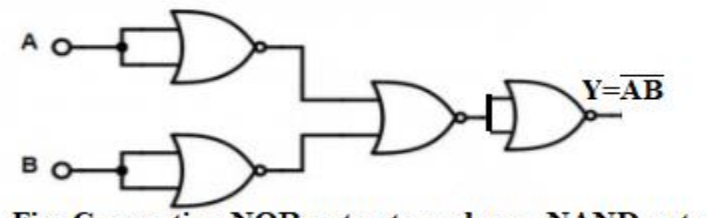


Fig: Connecting NOR gates to make an NAND gate

The above diagram is of an NAND gate made from combinations of NOR gates, arranged in a proper manner. The truth table of an NAND gate is also given beside the diagram.

- **Implementing X-OR Gate Using only NOR Gates**

An X-OR gate can be replaced by NOR gates as shown in the figure.

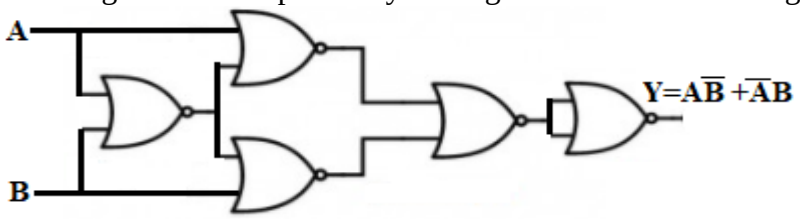


Fig: Connecting NOR gates to make an X-OR gate

The above diagram is of an X-OR gate made from combinations of NOR gates, arranged in a proper manner. The truth table of an X-OR gate is also given beside the diagram.

- **Implementing X-NOR Gate Using only NOR Gates**

An X-NOR gate can be replaced by NOR gates as shown in the figure.

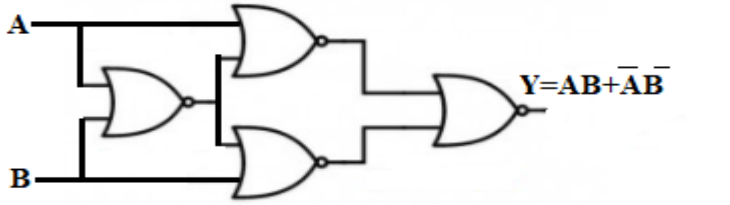


Fig: Connecting NOR gates to make an X- NOR Gate

The above diagram is of an X-NOR gate made from combinations of NOR gates, arranged in a proper manner. The truth table of an X-NOR gate is also given beside the diagram.

Logic Family:

Different Types of logic gates family are:

i. RTL: Resistor Transistor Logic
ii. DCTL: Direct Coupled Transistor Logic
iii. RCTL: Resistor Capacitor Transistor Logic
iv. DTL: Diode Transistor Logic
v. TTL: Transistor Transistor Logic
vi. IIL: Integrated Injection Logic

Various types of gates are involved in logic gates family. Among them, here we described only RTL and TTL gates.

RTL and TTL (Resistor Transistor Logic and Transistor Transistor Logic)

You can give an example preferably for NOR and NAND gate because both gate are Universal Gate.

RTL: Resistor transistor logic gate family is often found in an IC. In which all the logic are implemented using resistor and transistors. One basic thing about the transistor (NPN), is that HIGH at input causes output to be LOW (i.e. like a inverter). In the case of PNP transistor, the LOW at input causes output to be HIGH.

An example of RTL gate is shown in figure, which implements the NOR function.

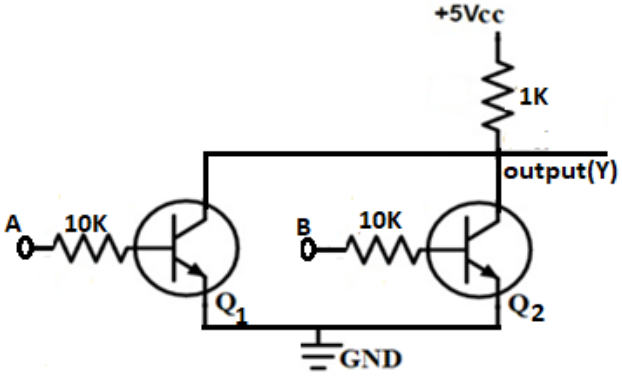


Fig: NOR gate using transistor

Working: The circuit arrangement is as shown in fig. It consists of two transistor Q_1 & Q_2.

- **If A=0, B=0:** Both Q_1 & Q_2 are at cut off condition, all Vcc current or voltage [power supply] goes to output so output remains high [1].
- **If A=0, B=1:** Q_1 is cut off and Q_2 is saturated, all Vcc current goes to GND through Q_2, so output remains low [0].
- **If A=1, B=0:** Q_2 is cut off and Q_1 is saturated, all Vcc current goes to GND through Q_1 so output remains low [0].
- **If A=1, B=1:** Both Q_1 & Q_2 are at saturated condition, all Vcc current or voltage [power supply] goes to GND through Q_1 & Q_2 so output remains low [0].

Definition of Transistor Transistor Logic (TTL):

Transistor-transistor logic (TTL) is a digital logic design in which bipolar transistors (BJT) and resistors. It is called transistor–transistor logic because both the logic gating function and the amplifying function are performed by transistors. TTL is notable for being a universal integrated circuit (IC) family used in many applications such as computers, industrial controls, test equipment and instrumentation, consumer electronics, synthesizers, etc.

An example of TTL gate is shown in figure, which implements the NAND function.

Circuit operation of NAND Gate using Transistor Transistor Logic [TTL]:

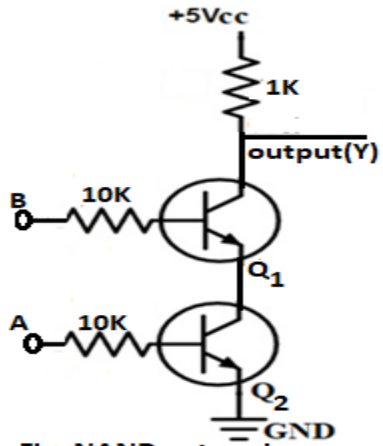


Fig: NAND gate using Transistor

- **If A=0, B=0**, Both Q_1 & Q_2 are at cut off condition, all Vcc current or voltage [power supply] goes to output so output remains high [1].
- **If A=0, B=1,** Q_1 is cut off and Q_2 is saturated due to Q_1 all Vcc current goes to Output so that output will be high [1].
- **If A=1, B=0,** Q_2 is cut off and Q_1 is saturated due to Q_2 all Vcc current goes to output so that output will be high [1].
- **If A=1, B=1,** Both Q_1 & Q_2 are at saturated condition, all Vcc current or voltage [power supply] goes to GND through Q_1 & Q_2 so that output will be low [0]

Working:

The circuit arrangement is as shown in fig. It consists of two transistor Q_1 & Q_2.

Circuit Operation of OR Gate Using Transistor Transistor Logic (TTL):

TTL or transistor transistor logic is the saturated logic circuit because it operates between cut-off [reverse biased] and saturation [forward biased]. During cut-off, the base current is zero, the base emitter junction is no forward biased and transistor doesn't conduct any current. During saturation, collector current is high and collector base junction is no reverse biased and transistor is conducting current.

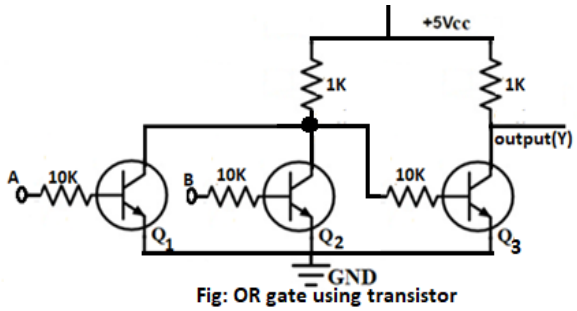


Fig: OR gate using transistor

Working: The circuit arrangement is as shown in fig. It consists of three transistor Q_1,Q_2 & Q_3.

- If A=0, B=0: Both Q_1 & Q_2 are at cut off condition, all Vcc current or voltage [power supply] goes to Q_3 and Q_3 is at saturated condition thus all current goes to GND so output remains low [0].
- If A=0, B=1: Q_1 is cut off and Q_2 is saturated, all Vcc current goes to GND through Q_2 i.e. base current of Q_3 is low i.e. Q_3 is cut off condition so that output will be high [1].
- If A=1, B=0: Q_2 is cut off and Q_1 is saturated, all Vcc current goes to GND through Q_1 i.e. base current of Q_3 is low i.e. Q_3 is cut off condition so that output will be high [1].
- If A=1, B=1: Both Q_1 & Q_2 are at saturated condition, all Vcc current or voltage [power supply] goes to GND and Q_3 is at cut off condition thus all current goes to output and output remains high [1].

Circuit operation of AND Gate using Transistor Transistor Logic [TTL]:

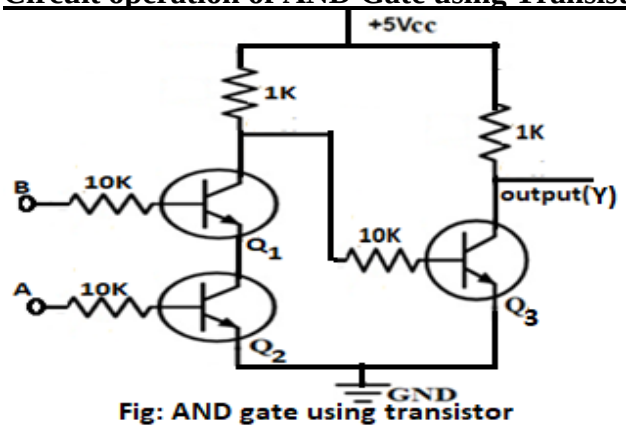


Fig: AND gate using transistor

Working: The circuit arrangement is as shown in fig. It consists of three transistor Q_1,Q_2 & Q_3.

- If A=0, B=0: Both Q_1 & Q_2 are at cut off condition, all Vcc current or voltage [power supply] goes to Q_3 and Q_3 is at saturated condition thus all current goes to GND so output remains low [0].
- If A=0, B=1: Q_1 is cut off and Q_2 is saturated, all Vcc current goes to Q_3, i.e. base current of Q_3 is high so Q_3 is saturated condition thus all current goes to GND through Q_3 so that output will be low [0].
- If A=1, B=0: Q_2 is cut off and Q_1 is saturated, all Vcc current goes to Q_3, i.e. base current of Q_3 is high so Q_3 is saturated condition thus all current goes to GND through Q_3 so that output will be low [0].
- If A=1, B=1: Both Q_1 & Q_2 are at saturated condition, all Vcc current or voltage [power supply] goes to GND through Q_1 & Q_2 i.e. base current of Q_3 is low so Q_3 is cutoff condition thus all current goes to output and output remains high [1].

Circuit operation of NOT Gate using Transistor Transistor Logic [TTL]:

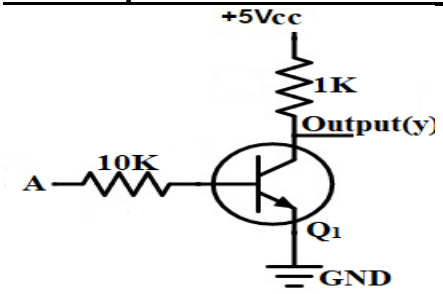


Fig: Circuit diagram of NOT gate using TTL

Working:

When A=0: Base input of Q_1 is low, Q_1 is cutoff so that supply is blocked by Q_1 all Vcc current and voltage goes to output and hence it remains as output high [1]

When A=1: Base input of Q_1 is high, Q_1 is saturated so that supply is blocked by Q_1 all Vcc current and voltage goes to GND and hence it remains as output low [0].

Advantage of TTL Gate:

- The propagation delay for a TTL gate is about 10nSec ($10x10^{-9}$Sec) as compared with 25nSec for the DTL and RTL.
- The noise immunity is batter for the TTL gate than RTL and DTL gates.
- With some simple modifications, the fanout of this TTL gate can be as great at 15 but for RTL gate is typically 5 and for DTL gate is 8.

Memory device:

The electronic circuits whose output remains as set until something is done to change it is called memory device.

FLIP – FLOPS

A positive signal feedback is used, resulting in two stable output states than can represent the two logic level 1 and 0. The circuit is placed in either state and remains in that state indefinitely until the input is changed. It stores a binary bit (1 or 0). There are various types of flip flop. They are

1. Reset-set (RS) flipflop
2. Data flipflop
3. JK flipflop

R-S Flip Flop[Re-set Set Flip Flop] and it's operation :

Flip-flop is a basic digital memory circuit having two stable and complementary outputs Q and $\overline{Q}$ Complementary means that, when Q=0, $\overline{Q}$ =1 and when Q=1, $\overline{Q}$ =0.

Flip-flops are the basic building blocks for counters, timer, resistors etc. The flip flops are often called ''Latcls'' as they hold or Latch in either stable state.

R-S Flip-flops (Latch)

R-S flip-flop consists of two inputs R and S and two outputs Q and $\overline{Q}$. The logic symbol of RS flip-flop is given as:

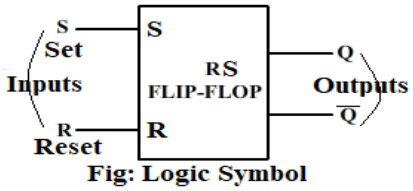


Fig: Logic Symbol

R-S flip-flop may be constructed by using NOR gate as well as NAND gate.

a. **By using NoR gate**

R-S flip-flop can be constructed by using two NoR gates as shown in the figure.

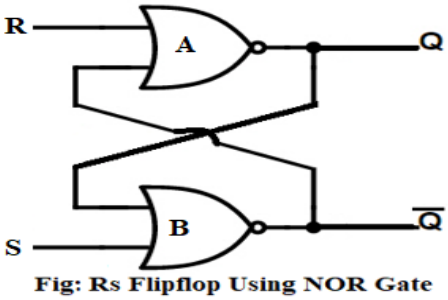


Fig: Rs Flipflop Using NOR Gate

R&S------inputs Q&$\overline{Q}$ ---------Outputs

Inputs		Outputs		Comments
R	S	Q	$\overline{Q}$	
0	0	Last state	No change	Nochange
0	1	1(Set)	0	Set
1	0	0	1 (Reset)	Reset
1	1	Illegal	Forbidden	Forbidden

Operation:

The operation of NOR gate RS flipflop is explained as follows operation, there arises 4 case as:

Case I : If R=0 , S= 0

In the first input condition i.e. R=0, S=0 as NOR gate is high sensitive, the output remains unchanged ie. Output of last state remains.

Case II : If R=0 , S= 1

When R=0, S=1 the NOR gate B (being high sensitive) gives low output ie. $\bar{Q} = 0$. Now both inputs of NOR gate A are low and hence the output is high i.e. Q=1. Therefore at S=1, R=0 the flipflop is said to be set.

Case III : If R=1 , S= 0

When R=1, S=0 the NOR gate A gives low output (i.e. Q=0). Hence both inputs of NOR gate B are low and hence its output is high i.e. $\bar{Q} = 1$. Therefore at R=1, the flipflop is said to be reset state.

Case IV : If R=1 , S= 1

When S=1, R=1. This is forbidden state because at this condition both the outputs Q & $\bar{Q}$ are low at the same time. This violates the basic principle of flipflop (Q & $\bar{Q}$ must be complementary of each other). So, we don't impose such condition. Incidentally if such condition is imposed result is unpredictable.

b. By Using NAND Gate:

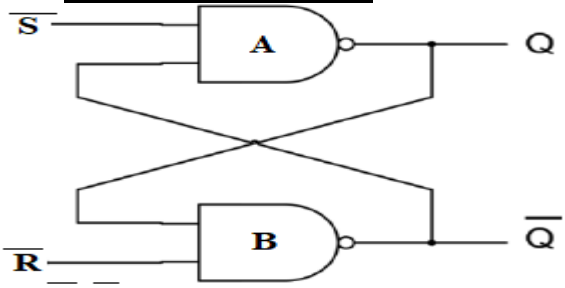
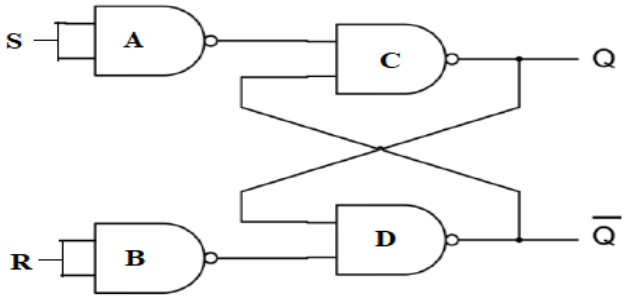


Fig: $\bar{R}$-$\bar{S}$ flip-flop using NAND Gate

Inputs		Outputs	
$\bar{R}$	$\bar{s}$	Q	$\bar{Q}$
0	0	Forbidden	Forbidden
0	1	0 Reset	1
1	0	1	Set
1	1	Last State	No change



Inputs		Outputs	
R	S	Q	$\bar{Q}$
0	0	Last State	No change
0	1	1 Set	0
1	0	0	1 Reset
1	1	Illegal	Forbidden

Figure2: R-S Flip Flop Using NAND Gate

To form a RS flipflop we connect two single input NAND gates A and B with the double input NAND gates C and D as shown in the second figure above.

The operation of NAND gate RS flipflop is explained as follows operation, there arises 4 case as:

Case I: If S=0, R=0

This makes $\bar{S} = 1$ and $\bar{R} = 1$. Since NAND gate is low sensitive output of NAND gates C and D remains unchanged. So, output of previous state is obtained.

Case II: If S=1, R=0

In this case $\bar{S}$ =0 and $\bar{R}$=1. Since output of NAND gate C is high i.e. Q=1, this makes inputs for NAND gate D both high, So, its output is low i.e. $\bar{Q}$ =0. This is called set state.

Case III : If S=0, R=1

In this case $\bar{S} = 1$ and $\bar{R} = 0$. This makes output of D high i.e. $\bar{Q}$ =1, this makes inputs for NAND gate C both high, So, it's output is low i.e. Q=0. This is called Reset State.

Case IV: If S=1, R=1

In this case $\bar{S} = 0$ and $\bar{R} = 0$. Thus, output of both NAND gates C and D are high i.e. Q=1 and $\bar{Q}$ =1, which violates the basic principle of flip flop. Thus, this state is forbidden state.

D-flip-flop or Data Flip Flop: What is the drawback of R-S flip flop that leads to the D-flip flop?

The RS flip flop has two data inputs S and R. To store high bit (i.e. Q=1), S must be high (1) and to store low bit (i.e. Q=0) R must be high. The generation of two signal to drive flip flop is inconvenient in many application. Further the forbidden condition any occur. This is the drawback that leads to the D-flip-flop.

Description of D-flip-flop [Clocked]:

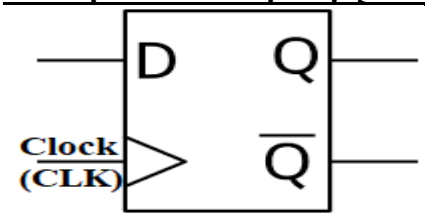


Fig: Logic Symbol of D flip flop

CLK	D	Q_{n+1}
0	Any (*)	Q_n Last state
1	0	0
1	1	1

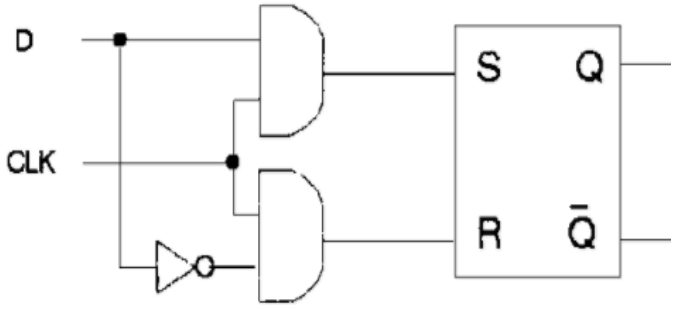


Fig: Block Symbol of D flip flop

The logic symbol diagram for D flip flop are as shown in fig above.

When clock (CLK) is low (0), the latch flip flop is disable and D can change the value without affecting Q i.e. Q remains in it's last state Q_n. When the clock is high, the latch is enabled and Q is equal to the value of D. When the clock is Q again low, Q stores the last value of D. In this way D flip flop works as the modified form of RS flipflop. The truth table for D flip flop is as shown above.

JK Flip Flop:

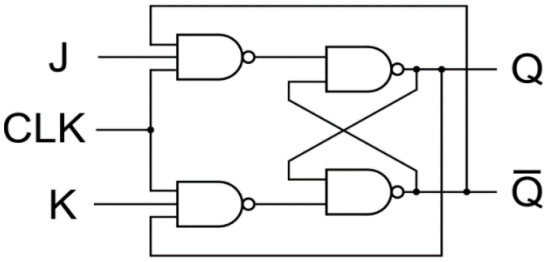


Fig: Logic Symbol of JK Flip flop

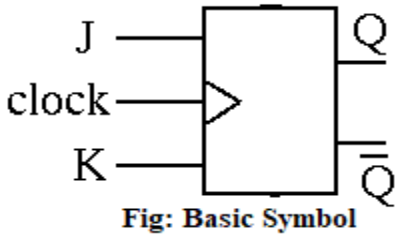


Fig: Basic Symbol

The above figure shows the logic diagram of JK Flip flop. Here, J and K are control input because they determine what the flip flop does when positive edge clock arrives.

Since the circuit is positive edge-trigger because of AND gate, it converts rectangular waves into spikes.

The function of JK flip flop can be explained in the following four cases:

Case I: When J=0 and K=0: In this case, the AND gates are disable. The clock gets don't Care condition. Therefore the output remains in the last state.

Case II: When J=0 and K=1: In this case, the upper AND gate is disabled. Hence there is no way to set the flipflop. The only possibility is to reset it. When next +Ve clocks arrives, lower posses a reset pulse. This makes the high Q low. This state is called reset state

Case III: When J=1 and K=0: In this case the lower gate is disabled. So it is impossible to reset the flipflop. But we can set it. When Q is low, $\bar{Q}$ is high, the upper gate passes a set signal in the next +Ve edge clock. Thus Q becomes high and $\bar{Q}$ becomes low i.e. when J=1 and K=0, the next +ve trigger of clock sets the flip flop.

Case IV: When J=1 and K=1: In this case, it is possible to set or reset the flip flop. If Q is high, lower gate passes a reset signal on the next positive trigger. When Q is low, upper gate passes a set signal on next positive trigger. Thus Q changes to the complement of the last state. So, when J=1, K=1, flip flop will toggle on the next positive trigger.

The corresponding truth table is given as:

CLK	J	K	Q_{n+1}	$\overline{Q_{n+1}}$	Comment
Don't care (*)	0	0	Q_n	$\overline{Q_n}$	Last state
High	0	1	0	1	Reset
High	1	0	1	0	Set
High	1	1	$\overline{Q_n}$	Q_n	Toggle
Low	Don't care (*)	Don't care (*)	Q_n	$\overline{Q_n}$	No change

Clock Circuits:

A clock is a circuit that produces periodic pulse. These pulse can be used to drive the different gates in the digital instrument. A clock can be constructed with a multivibrator whose output states are unstable and as a consequence has an output signal that changes periodically between high and low.

Multivibrators:

The oscillator which produce the output of square wave, rectangular, saw tooth, triangular type then, such type of oscillator are called multivibrators. They are used to generate pulse such that counting circuit, digital circuit, switching circuit etc can be operated. Those types of multivibrators, the output is changed discontinuously. These circuits are called two stage amplifier because one transistor is used to operate other. There are three types of multivibrators, they are,

a. Astable multivibrators:
- It has no stable state but only two quasistable (half stable) states.
- It has two energy storing elements.

b. Monostable multivibrators
- It has one stable state.
- It has one energy storing element.

c. Bistable multivibrators
- It has two stable state.
- It has no energy storing element.

❖ **Uses of multivibrators:**
- As frequency dividers.
- As sawtooth generators.
- As square wave and pulse generator.
- For many specialized uses in radar and TV circuits.
- As memory elements in computers.

a. Astable multivibrators (working principle of astable multivibrator)

Figure shows the circuit of an astable multivibrator consisting two identical transistor Q_1 and Q_2. It is a two stage RC coupled amplifier. The output of each stage is coupled to the input of the other through a capacitor (C_1 & C_2). It, in fact, consists of two CE amplifier stages, each providing a feedback to the other. The feedback ratio is unity and positive because of 180^0 phase shift in each stage. Hence, the circuit oscillates. Because of the very strong feedback signal, the transistors are driven either to saturation or cut-off. They do not work on the linear region of their characteristics.

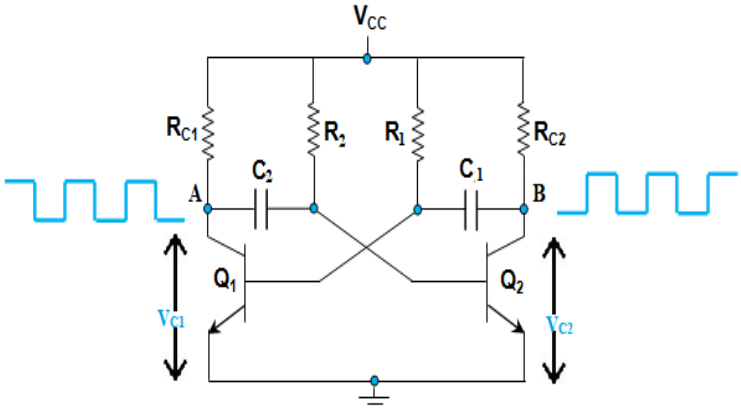


Fig: Astable Multivibrator Using BJTs

When power V_{CC} is applied, then collector current starts flowing in Q_1 & Q_2. The coupling capacitor C_1 & C_2 start charging up. The characteristics of two similar transistor can be exactly alike. i.e.

- When Q_1 is ON , Q_2 is OFF
- When Q_2 is ON, Q_1 is OFF

Suppose that Q_1 starts conducting before Q_2. The feedback system in such that Q_1 will be very rapidly driven to saturation and Q_2 to cut off. The circuit operation may be explained as follows:

- Since Q_1 is in saturation whole of V_{cc} drops acrossR_{C_1}. Hence $V_{C_1} = 0$ and point A is at zero or ground potential.
- Since Q_2 is in cut off i.e. it conducts no current, there is no drop across R_{C_2}. Hence point B is at V_{cc}.
- Since A is at 0V, C_2 starts to charge through R_2 towards V_{CC}.
- Capacitor C_2 now begins to discharge which decreases the reverse bias on base of Q_2. Therefore Q_2 begins to conduct. Consequently, collector of Q_2 becomes less positive. This negative going voltage signal is applied to base of transistor Q_1 through the capacitor C_1. Which result, Q_1 to cutoff simultaneously Q_2 to saturation. Now V_{C_2} decreases to zero when Q_2 gets saturation. Consequently, potential at B decreases from V_{CC} to almost zero.

The transistor Q_1 remains cutoff and Q_2 in conducting until C_1 discharging through R_1, enough to decreases the reverse bias of Q_1. The whole cycle repeats.

The output taken from the collector of either transistor is shown in graph.

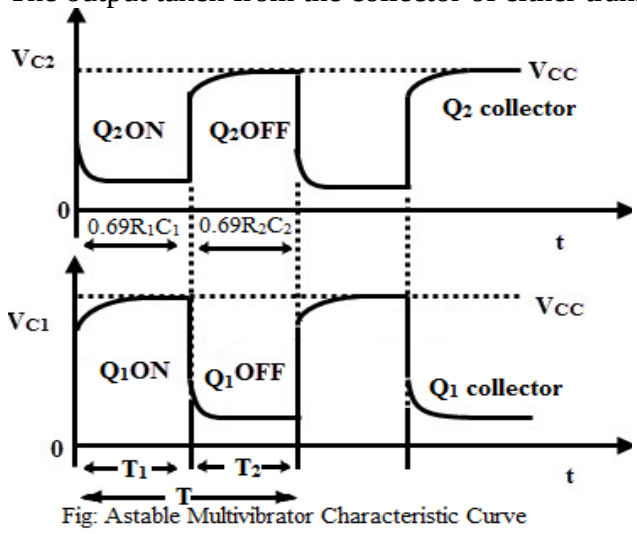


Fig: Astable Multivibrator Characteristic Curve

The multivibrator circuit alternates between a state in which Q_1 is ON and Q_2 is OFF and a state in which Q_1 is OFF and Q_2 is ON.

ON time for Q_1, $T_1=0.693R_1C_1$

ON time for Q_2, $T_2=0.693R_2C_2$

Total period $T= T_1+T_2 =0.693(R_1C_1+ R_2C_2)$

For symmetrical astable multivibrator i.e. $R_1= R_2$ and $C_1= C_2$

Then, $T =2\times0.693RC =1.38RC$

∴ Frequency of oscillation: it is given by the reciprocal of time period, $F = \frac{1}{T} = \frac{1}{1.38RC} = \frac{0.7}{RC}$

To specify how unsymmetrical the output is , we will use the duty cycle define as $D = \frac{W}{T} \times 100\%$

Monostable Multivibrator:

Multivibrators have two different electrical states, an output "HIGH" state and an output "LOW" state giving them either a stable or quasi-stable state depending upon the type of multivibrator. One such type of a two state pulse generator configuration are called Monostable Multivibrators.

Monostable Multivibrators have only ONE stable state (hence their name: "Mono"), and produce a single output pulse when it is triggered externally. Monostable Multivibrators only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

Construction of Monostable Multivibrator

Two transistors Q_1 and Q_2 are connected in feedback to one another. The collector of transistor Q_1 is connected to the base of transistor Q_2 through the capacitor C_1. The base Q_1 is connected to the collector of Q_2 through the resistor R_2 and capacitor C. Another dc supply voltage $-V_{BB}$ is given to the base of transistor Q_1 through the resistor R_3. The trigger pulse is given to the base of Q_1 through the capacitor C_2 to change its state. R_{L1} and R_{L2} are the load resistors of Q_1 and Q_2.

One of the transistors, when gets into a stable state, an external trigger pulse is given to change its state. After changing its state, the transistor remains in this quasi-stable state for a specific time period, which is determined by the values of RC time constants and gets back to the previous stable state.
The following figure shows the circuit diagram of a Monostable Multivibrator.

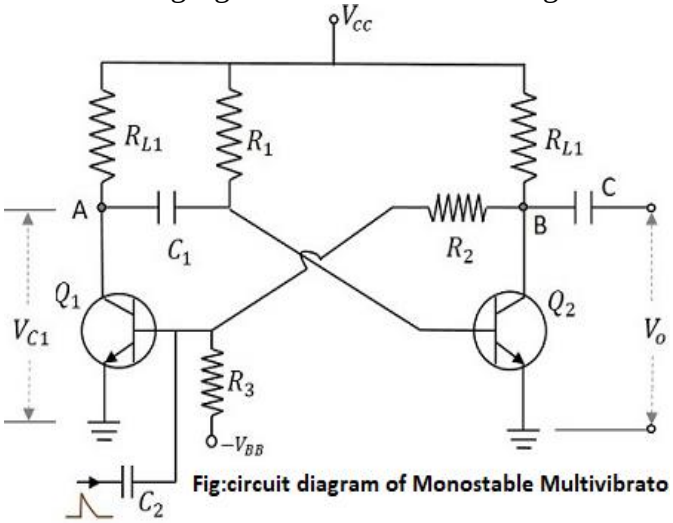


Fig:circuit diagram of Monostable Multivibrato

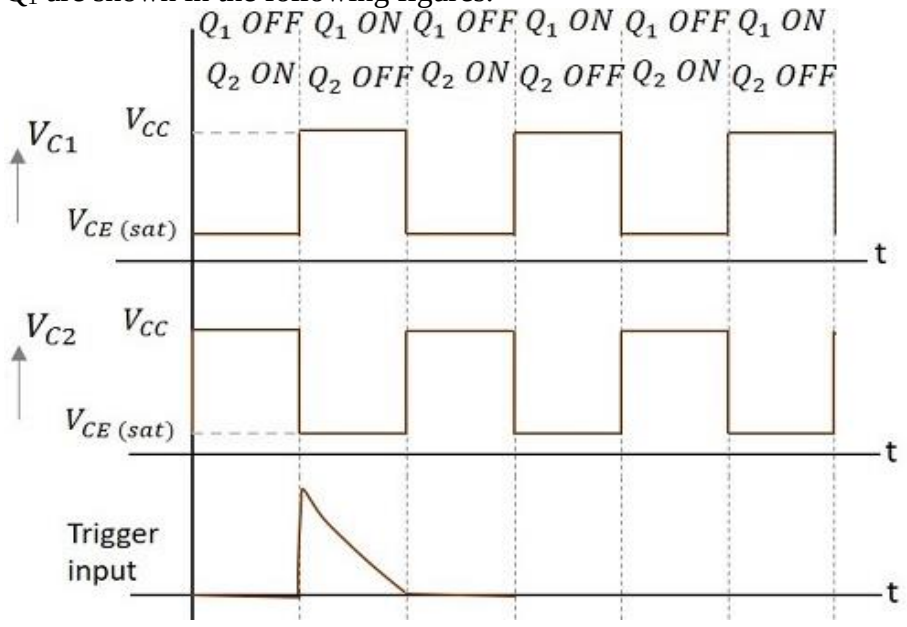
Operation of Monostable Multivibrator

Firstly, when the circuit is switched ON, transistor Q_1 will be in OFF state and Q_2 will be in ON state. This is the stable state. As Q_1 is OFF, the collector voltage will be V_{CC} at point A and hence C_1 gets charged. A positive trigger pulse applied at the base of the transistor Q_1 turns the transistor ON. This decreases the collector voltage, which turns OFF the transistor Q_2. The capacitor C_1 starts discharging at this point of time. As the positive voltage from the collector of transistor Q_2 gets applied to transistor Q_1, it remains in ON state. This is the quasi-stable state.

The transistor Q_2 remains in OFF state, until the capacitor C_1 discharges completely. After this, the transistor Q_2 turns ON with the voltage applied through the capacitor discharge. This turn ON the transistor Q_1, which is the previous stable state.

Output Waveforms

The output waveforms at the collectors of Q_1 and Q_2 along with the trigger input given at the base of Q_1 are shown in the following figures.



The width of this output pulse depends upon the RC time constant. Hence it depends on the values of R_1C_1. The duration of pulse is given by

$T=1.1RC$

The trigger input given will be of very short duration, just to initiate the action. This triggers the circuit to change its state from Stable state to Quasi-stable or Meta-stable or Semi-stable state, in which the circuit remains for a short duration. There will be one output pulse for one trigger pulse.

The Technology of Manufacturing Integrated Circuits

Introduction

Many of the technological achievements of the past two or three decades have been based on microelectronics. Microelectronics devices are at the heart of new products ranging from communication satellites to computers and space shuttles. The revolution in the electronic technology brought by microelectronics is mainly based upon the semiconducting materials.

Semiconductor Purification: Zone Refining

Zone refining technique is used to purify an element or compound or for the formation of a single crystal by melting a short region (i.e. zone) and causing this liquid zone to travel slowly through a relatively long ingot (An ingot is a piece of relatively pure material, usually metal) or charge (rod) of the solid. This process is based on a very important fact that the solid to crystallize first from the melt is purer element to be obtained than the liquid. Silicon and Germanium are two of the most widely used semiconductor materials. Out of these two, Si has wide spread use because of various factors associate with the material.

i. It is easy for doping by impurities.
ii. Silicon has efficient response to solar radiation and light.
iii. Silicon has relatively high dielectric strength and therefore suitable for power devices.
iv. The raw material from which pure silicon is found everywhere in nature. So it is very cheap.
v. The energy gap of silicon is moderate leading to small leakage current.
vi. It is most abundant element after oxygen in the earth. About 27.6% of the earth's crest is made up of silicon.

The Single Crystal Growth

The production of even the simplest of ICs is complex, time consuming, and prone to defects. Despite this, highly sophisticated ICs can be produced at reasonable cost. One of the main reasons is that methods have been developed in the last few decades for growing large single crystals of Si, thereby permitting mass production. By processing several wafers simultaneously, the cost of the individual IC is minimized. We will now discuss some of the methods used for single-crystal growth.

1. The Czochralski Method:

One of the techniques commonly used to grow single-crystal silicon consists in dipping a small seed crystal of Si into a crucible containing the molten silicon. The seed is then slowly raised from the melt. As the seed is lifted away from the melt a single crystal grows continuously onto the seed. A schematic of this method; known as the Czochralski method is shown in Fig. To average any variations in the temperature of the melt and thus ensure uniformity in the growing crystal, the crystal is rotated slowly (a few revolutions per minute) as it is being raised. The conditions needed for good single-crystal growth are initially determined by trial and error. For example, the rate at which the growing crystal is raised is a crucial factor, and a few millimeters per hour is a fairly typical rate. Once these growing conditions are determined, they can be readily reproduced.

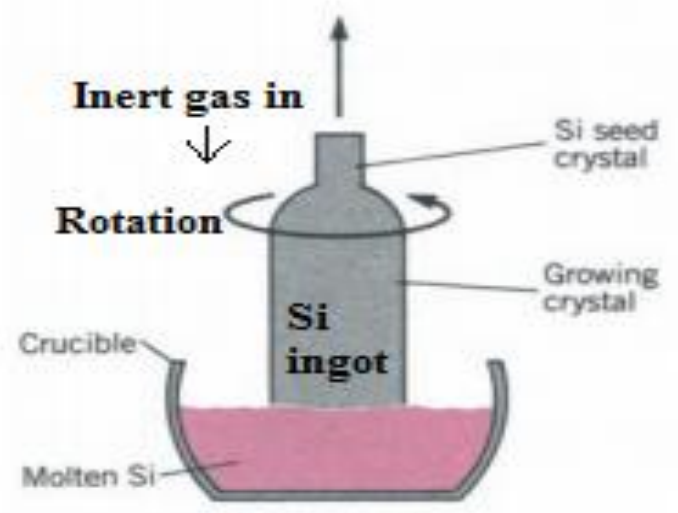


Figure: Schematic diagram of the Czochralski method for growing single crystals.

2. The Bridgman Stockbarger Method:

Another method used for growing single crystals, called the Bridgman-Stockbarger method, is shown in Fig. The material is placed in a crucible having a conical tip. The sample, which is initially polycrystalline, is first melted in an upper furnace that is maintained a few degrees above the melting point. The crucible is then slowly lowered into a second furnace with a temperature a few degrees below the melting point. As the crucible enters this lower furnace, a small crystal is formed at the tip of the crucible. This crystal acts then as the seed for the rest of the melt and, as the crucible continues to be lowered, a single crystal is grown.

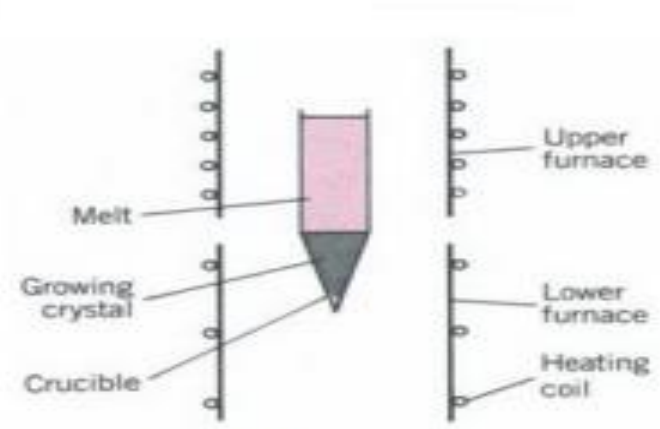


Figure:
Schematic diagram of the Bridgman-Stockbarger method for growing single crystals.

3. Floating Zone Method:

The two methods just described have the disadvantage that the melt tends to dissolve some of the oxygen from the walls of the crucible (usually made of silica, SiO_2, which has a higher melting point than silicon). The solution to this problem is found in the floating zone method, which dispenses with the crucible altogether. A schematic of the arrangement used in the floating zone method is shown in Fig. A polycrystalline rod of the crystal to be grown is held between two support posts inside a furnace filled with an inert gas. A small seed crystal is placed between the lower support post and the rod. A small molten zone is created at the end of the rod in contact with the seed by means of a moveable external heating coil. As the coil is slowly raised, the molten zone moves upward, while the crystal solidifying behind it grows onto the seed. The molten zone is held between the unmelted ends by surface tension. The floating zone technique is also used for zone refining.

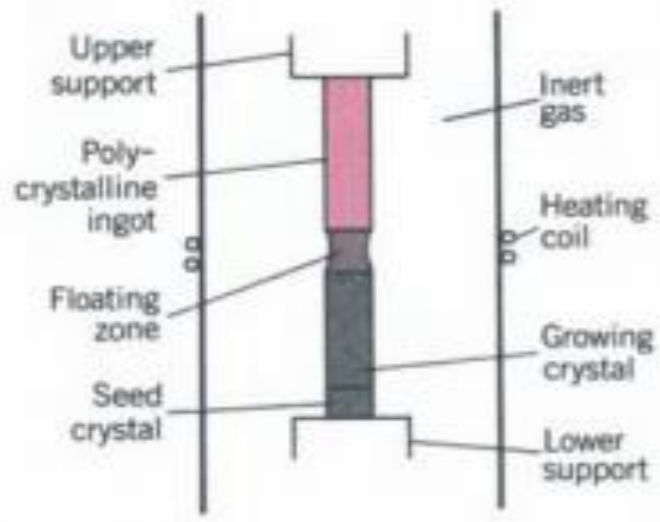


Figure:
Schematic diagram of the floating zone method for single-crystal growth.

4. <u>Epitaxy:</u>

A crystal-growing method that plays an important role in the fabrication of ICs is vapor-phase epitaxy. Very often the whole integrated circuit is made on a layer of Si, which is grown epitaxy onto a Si substrate (wafer). In this method, atoms of Si from a vapor are deposited on the substrate in a layer that has the same crystal structure and orientation as the substrate. Thus, the substrate serves as the seed crystal onto which the epitaxy layer grows. This first layer in turn serves as the substrate for the second layer, and so on. A schematic of the apparatus used for vapor epitaxy is shown in Fig. Single crystal wafers of Si are

placed in a heated chamber called the "reactor." Gaseous compounds of silicon (for example, silicon tetrachloride, SiC4), together with the appropriate reactant gas, are introduced into the reactor chamber. The temperature of the reactor is adjusted to produce the reaction that will liberate the silicon by decomposition of the compound. Thus, for example, at 1250°C the reaction $SiCl_4 + H_2 \rightarrow Si + HCl$ occurs. Some of the Si atoms released in the reaction are deposited onto the silicon substrates, thereby forming epitaxial layers. If the chemicals used for the reaction are of high purity, the epitaxial layer of Si will be highly pure. Alternatively, the layer can be deliberately doped, making it either p-type or n-type, by passing the hydrogen through a solution containing boron or phosphorous atoms (for example, boron trichloride or phosphorous trichloride), before it is introduced into the reactor.

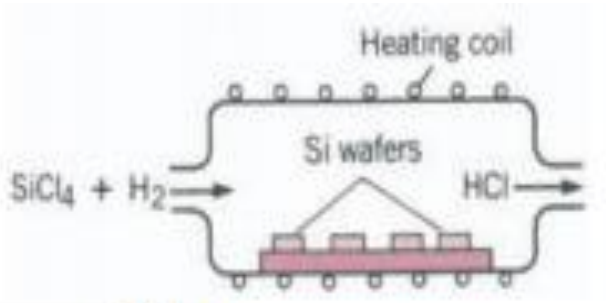


Figure: Arrangement for growing Si layers on silicon wafers by epitaxial growth.

The Process of IC Production:

The processes involved in the fabrication of integrated circuits include epitaxial growth, oxidation, oxide removal and pattern definition, doping (introduction of selective impurities in the Si), and interconnection of components. We will now explain the additional steps in the manufacturing of integrated circuits.
The processes involved in the fabrication of integrated circuits are as follow;

1. Photolithography
2. Doping
3. Metallization

They are describe below;

1. Photolithography

Photo means light, Litho means stone and Graphy means write. Photolithography is the standard method of printed circuit board (PCB) and microprocessor fabrication. The process uses light to make the conductive paths of a PCB layer and the paths and electronic components in the silicon wafer of microprocessors. It involves following steps.

a. Coat Si with oxide then with photoresist (Oxidation)

A key step in the production of an IC is the formation of a silicon dioxide ($Si0_2$) layer on the surface of the silicon. The oxide layer also protects *p-n* junctions from contamination. Finally, because $Si0_2$ is nearly an insulator, the oxide allows the interconnection of the circuit components by means of thin aluminum strips without short-circuiting sections of the IC. The oxide layer is grown by heating the silicon wafer to temperatures ranging between lOOO°C and 1200°C in an atmosphere of either pure oxygen or steam. The thickness of the oxide layer depends on the oxidation time and the temperature and the composition of the atmosphere in which the oxidation is performed. By careful selection of these three parameters, the exact thickness of the layer can be controlled. A layer 0.1 μm thick can be grown in one hour, at T = 1000°C, in pure oxygen. In the same time, a layer 0.5 μm thick grows in a steam environment.

b. Expose to radiation and develop the patter (Pattern Definition)

To make an integrated circuit, a method of creating accurate patterns on the silicon wafer is needed. *Photolithography* (or *masking)* allows the removal of the silicon dioxide in the desired sections of the wafer. Once these "windows" have been opened, diffusion of dopants or deposition of metallic contacts

can be performed. The process of photolithography is carried out as follows. The oxidized wafer is coated with a thin layer of a photosensitive material called *photoresist.* This is done by placing a drop of a solution containing the photoresist on the wafer. A thin film is then formed by spinning the wafer very rapidly. Finally, the wafer is heated to speed up the evaporation of the solvent and to enhance the adhesion of the photoresist film to the oxide layer.

A mask with the desired pattern is then placed on the photoresist film. The wafer is exposed to ultraviolet light that changes the structure of the exposed photoresist so that the exposed and unexposed parts have different solubility in certain chemical solutions. Thus, exposure to the ultraviolet light, followed by development in the appropriate chemical solution, allows the removal of the unexposed section of the photoresist. The sections of the silicon dioxide layer not protected by the photoresist are then etched away in a solution of **Hydrofluoric Acid (HF),** which selectively attacks the $Si0_2$ while leaving the photoresist and the silicon intact. After the window pattern has been opened in the $Si0_2$, the remaining **photoresist** is washed away with the appropriate solvent. The wafer is now ready for the introduction of the dopants or for the evaporation of metallic contacts. The various steps involved in the formation of these "windows" are illustrated in Fig.

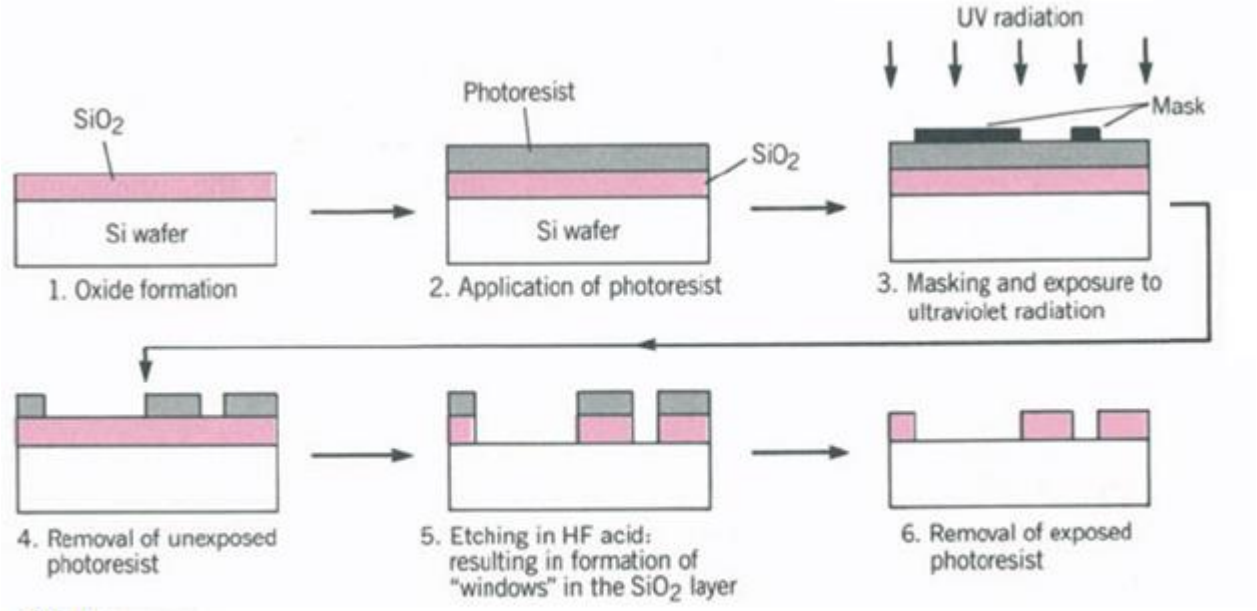


Figure:
Steps involved in the masking process (photolithography) used to open "windows" selectively on the silicon wafer.

2. Doping:

An integrated circuit has the named *chip*. The formation of circuit components in a chip is achieved by the selective introduction of donor and acceptor impurities into the Si wafer to create localized n-type and *p-type* regions. The two most commonly used techniques are as follows;

a. Diffusion:

When Si is heated to temperatures in the neighborhood of 1000°C, some of the semiconductor atoms move out of their lattice sites, leaving behind empty lattice sites that can migrate through the sample. If the heating is done in an atmosphere of either phosphorous or boron atoms, these impurity atoms move into the vacant lattice sites at the surface of the silicon and subsequently migrate slowly into the bulk of the Si with the assistance of the vacant lattice sites formed at high temperature. The diffusion of the dopant impurities can be stopped by cooling down the wafer. Because this solid state diffusion of impurities is time and temperature dependent, the depth of the diffusion layer can be controlled by varying these two

parameters. Another important aspect of the diffusion of either boron or phosphorous impurities is that at the same temperature they move much more slowly in $Si0_2$ than in pure Si. Thus, the oxide pattern, formed by the photolithographic method described earlier, acts as a mask that permits the diffusion of the impurities only in specific regions of the wafer. Above figure shows a schematic of a typical diffusion furnace used in the fabrication of Si chips. The dopants to be diffused into the silicon wafers are introduced into the heated furnace by means of an inert carrier gas that is bubbled through the molten dopant.

In general, diffusion systems are similar to oxidation furnaces. The dopant can be provided in the form of solid, liquid and gas.

i. Solid Source:

In this system, the dopant (doping) source is in solid form. The carrier gases O_2 and N_2 packs up the vapour from the dopant source and transport it to the furnace tube, where the dopant atoms are deposited on the surface of wafer.

- The common solid source of Boron is Trimethyl Borate

$2(CH_3O)_3B + 9O_2 \rightarrow B_2O_3 + 6CO_2 + 9H_2O$

$2B_2O_3 + 3Si \leftrightarrow 4B + 3SiO_2$

- The common solid source of Phosphorus is Phosphorous Pentoxide.

$2P_2O_5 + 5Si \leftrightarrow 4P + 5SiO_2$

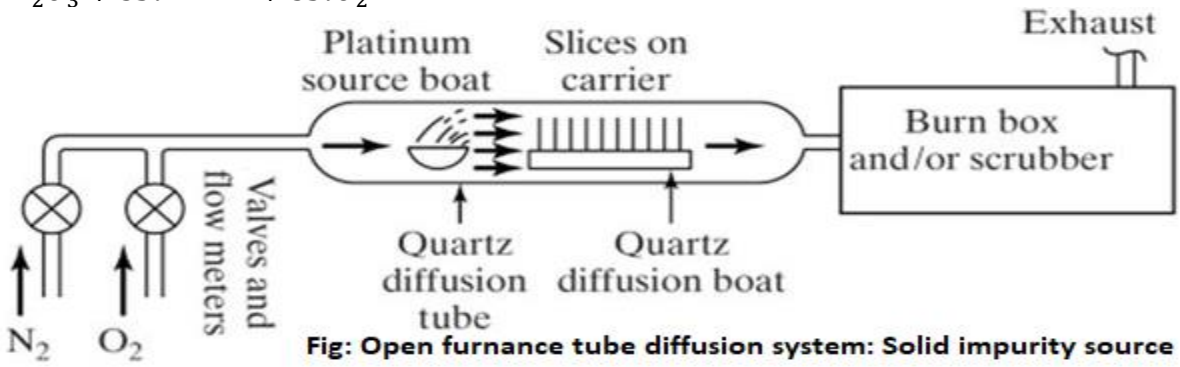


Fig: Open furnance tube diffusion system: Solid impurity source

ii. Liquid Source:

In this system, the dopant source is liquid form. The carrier gas passes through a bubbler where it picks up the vapour of the liquid source. The carrier gas carries vapour into the furnance tube where it reacts with the surface of the silicon wafer.

- The common liquid source of Boron is Boron Tribromide.

$4BBr_3 + 3O_2 \rightarrow 2B_2O_3 + 6Br_2$

$2B_2O_3 + 3Si \leftrightarrow 4B + 3SiO_2$

- The common liquid source of Phosphorus is Phosphorous Oxychloride.

$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2$

$2P_2O_5 + 5Si \leftrightarrow 4P + 5SiO_2$

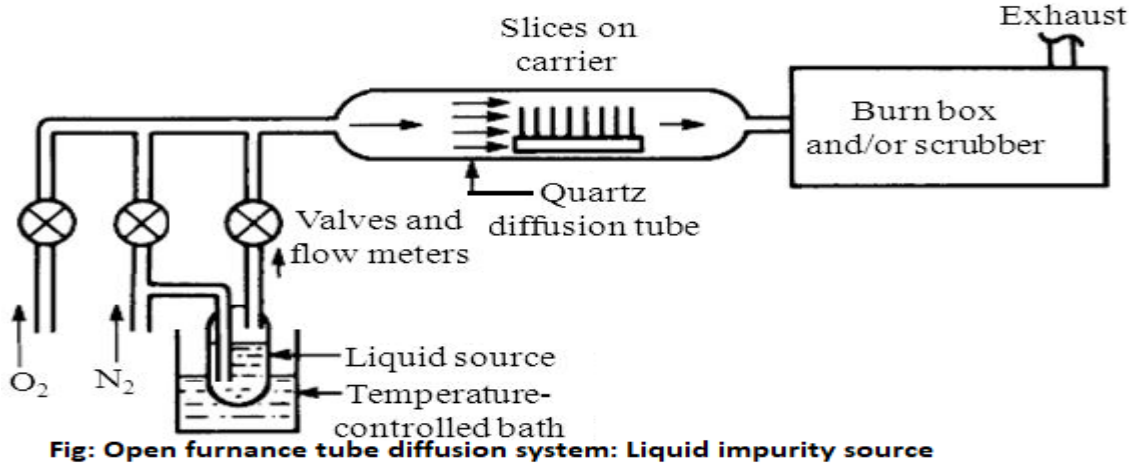


Fig: Open furnance tube diffusion system: Liquid impurity source

iii. Gas Source:

The dopants are directly supplied to the furnace tube in gas sources. The system is required to ensure that all the gas sources are removed from the system before entry or removal of safer because the common gas sources are extremely toxic.

- The primary gaseous source of Boron id Diborance.

$B_2H_6 + 3O_2 \rightarrow B_2O_3 + 3H_2O$

$2B_2O_3 + 3Si \leftrightarrow 4B + 3SiO_2$

- Phosphene is used as gaseous source for Phosphorus.

$2PH_3 + 4O_2 \rightarrow P_2O_5 + 3H_2O$

$2P_2O_5 + 5Si \leftrightarrow 4P + 5SiO_2$

For antimony, The solid source is Sb_2O_3 and Sb_2O_4 at the temperature of 900°C. The liquid source foor Sb is Sb_3Cl_5 in a bubbler. For Arsenic, the solid source is As_2O_3 and the gas source is AsH_3.

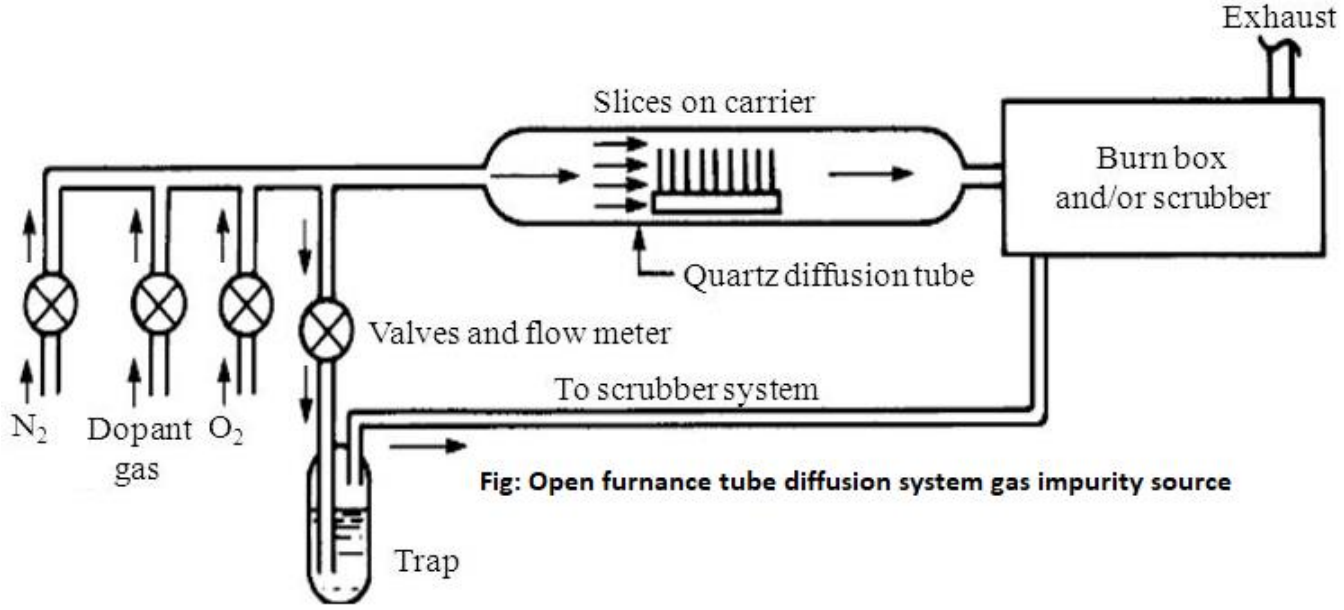


Fig: Open furnance tube diffusion system gas impurity source

b. Ion Implantation

It is an engineering process by which ions of a material are accelerated in an electric field and impacted into a solid. Ion implantation is used to change the physical, chemical and electrical properties of solid. It is used in semiconductor devices fabrication and in metal finishing as well as in various application of material science. The ion implantation system consists of;

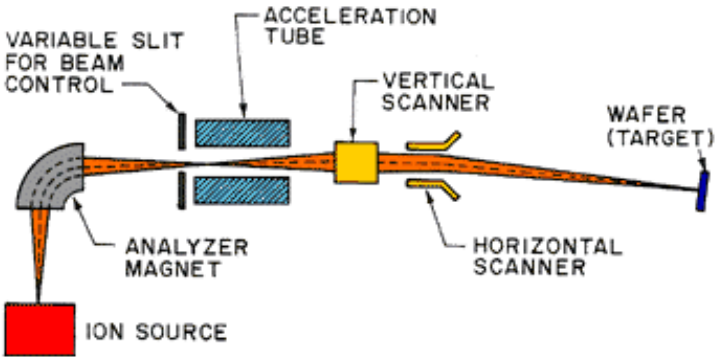
i. Ion source: Where plasma of desired impurity are produced.

ii. An accelerator: Where the ions are accelerated to high energy. The accelerating voltage may be form 20kV to as much as 250kV.

iii. A target chamber:

Where the ions impinge on a target which is the material to be implanted.

An analyzer magnet bends the ion beam through a right angle to select the required impurity ion. Scanning system consists of a vertical and horizontal scanner. Which provides necessary deflection to give a uniform implantation and to build up the desired dose. The diagram of ion implantor as shown as figure.



The centrifugal force is balanced by magnetic force,

$$Bqv = \frac{mv^2}{r}$$

$$B = \frac{mv}{r}$$

$$r = \frac{mv}{Bq} \text{.....i}$$

This means the impurities having different mass have different radius. This allows us to pass desired impurity species by providing slit on the path of beam. Also, the electrostatic energy provides necessary K.E. Therefore

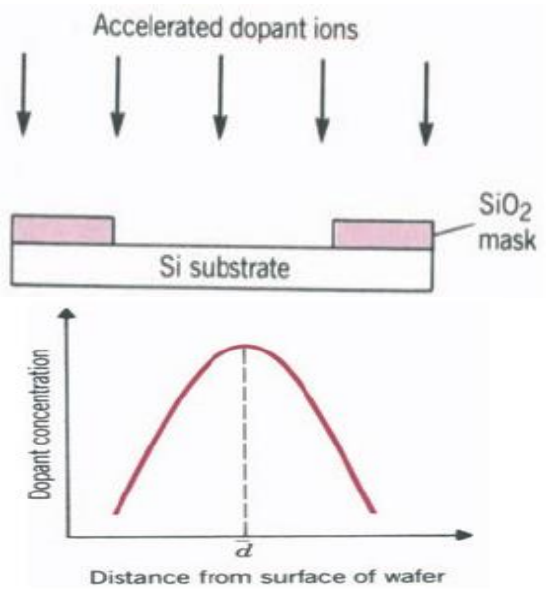
$$qV = \frac{1}{2}mv^2$$

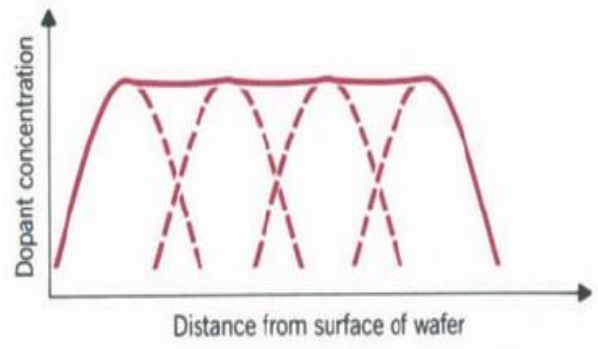
$$\therefore v = \sqrt{\frac{2qV}{m}} \dots\dots\dots\dots\dots\dots ii$$

Using equation ii in equation i we get,

$$B = \frac{mv}{qr} = \frac{m}{qr}\sqrt{\frac{2qV}{m}} = \sqrt{\frac{2qV}{m} \times \frac{m^2}{q^2r^2}}$$

$$\therefore B = \sqrt{\frac{2mv}{qr^2}} \dots\dots\dots\dots\dots\dots iii$$





Hence, the magnitude of magnetic field can be adjusted for a required ion of mass 'm'. The target chamber is maintained at relatively low temperature during the implantation which presents undersigned spreading of impurities by diffusion. It is very important in Very Large Scale Integration of VLSI fabrication.

The process ion implantation is performed at room temperature and has many advantages over diffusion. This permits the implantation of doped layers without disturbing previously implanted layers. As the impurities are ionized, they represent a current that can be measured very accurately. This allows accurate control of the impurity concentration. Ion implantation is used with the impurities which don't diffuse in Silicon easily. The recent use of arsenic as a dopant in MOS(metal oxide Semiconductor) devices is due to the advent of ion implantation.

Ion implantation follows a Gaussian distribution is given by,

$$N(x) = N_p e^{-\frac{(x-R_p)2}{2\Delta R_p}}$$

Where, $N(x)$ is the impurity concentration
N_p is the peak concentration
$R_{p\ is}$ the projected range
ΔR_p is the standard deviation called straggle

The following graph shows the result of varying acceleration voltage serval times during the implantation process. The gaussian disturbation represents a different accelerating potential. The solid line is obtained by summing up the individual Gaussian distribution and the sum as can be seen from the graph.

c. Connection of Components in a Chip (Metallization)

An IC chip consists of many superimposed doped layers. To complete the circuit, the electronic components within a layer as well as the layers themselves must be electrically connected. This can be done either by forming heavily doped (and therefore conductive) regions of silicon or by metal electrodes. This latter method is performed by metallic *thin film evaporation.* A schematic of the setup used for the evaporation of thin metallic films is shown in Fig. A charge of the metal to be evaporated (usually aluminum or gold) is placed in a crucible. The silicon wafers are placed above the crucible in a device called the *planetary*. Vapor of the metal is produced by heating the crucible with a heater coil wrapped around it, or by electron bombardment. As the metal vapor hits the cooled, masked wafer, it condenses on it, thus forming a thin metallic layer in a desired pattern that connects the different sections of the IC chip. The whole evaporation process is performed in a vacuum to avoid contamination of the metal vapor with the oxygen in the air.

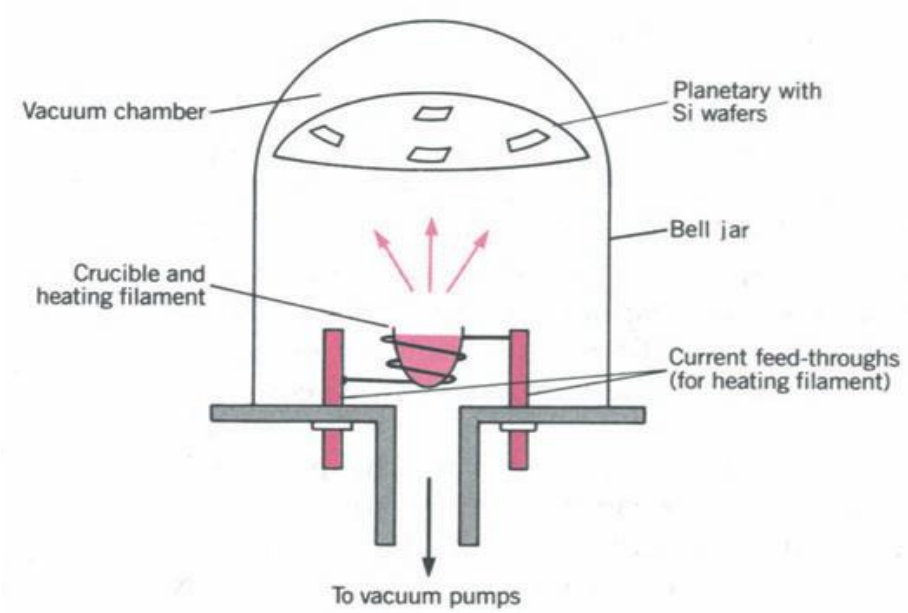


Figure: Schematic representation of a vacuum chamber used for vapor deposition of metallic interconnecting strips.

Electronic Component Fabrication of a Chip:

In this section we will illustrate how the techniques just described can be used to fabricate the basic components of a circuit: transistors, diodes, resistors, and capacitors. For simplicity, we will discuss the formation of each component separately. In the actual fabrication of an IC, parts of several components are formed simultaneously This will be illustrated at the end of this section, where we discuss how a simple gate can be made.

1. Transistor and Diodes:

The steps needed to build a bipolar transistor on a Si wafer are illustrated in Fig. 28-14.

a. An epitaxial (called an epilayer) n-type layer is grown onto a p-type wafer (Fig. 28-14a). Part of this layer will serve as the collector.
b. The n-type epilayer is then oxidized, masked, exposed to UV light, and so on, resulting in the formation of a window in the oxide layer (Fig. 28-14b).
c. Acceptor-type impurities are diffused to convert part of the exposed n-Iayer to p-type (Fig. 28-14c). A part of this p-type island will be the base of the transistor.

d. The wafer is again oxidized, a window is opened in the new oxide layer, and a diffusion of donor impurities is performed (Fig_ 28-14d), reconverting part of the p-type island to n-type. The latter region is the emitter of the transistor.
e. In the final step the wafer is reoxidized and three windows are opened: one into the collector, one into the base, and one into the emitter. Aluminum is evaporated to connect the three elements of the transistor (emitter, base, and collector) to other components of the circuit (Fig. 28-14e).

The steps needed to build a diode are identical to those used in the fabrication of a transistor except that the last diffusion of donor impurities (step 4) is omitted.

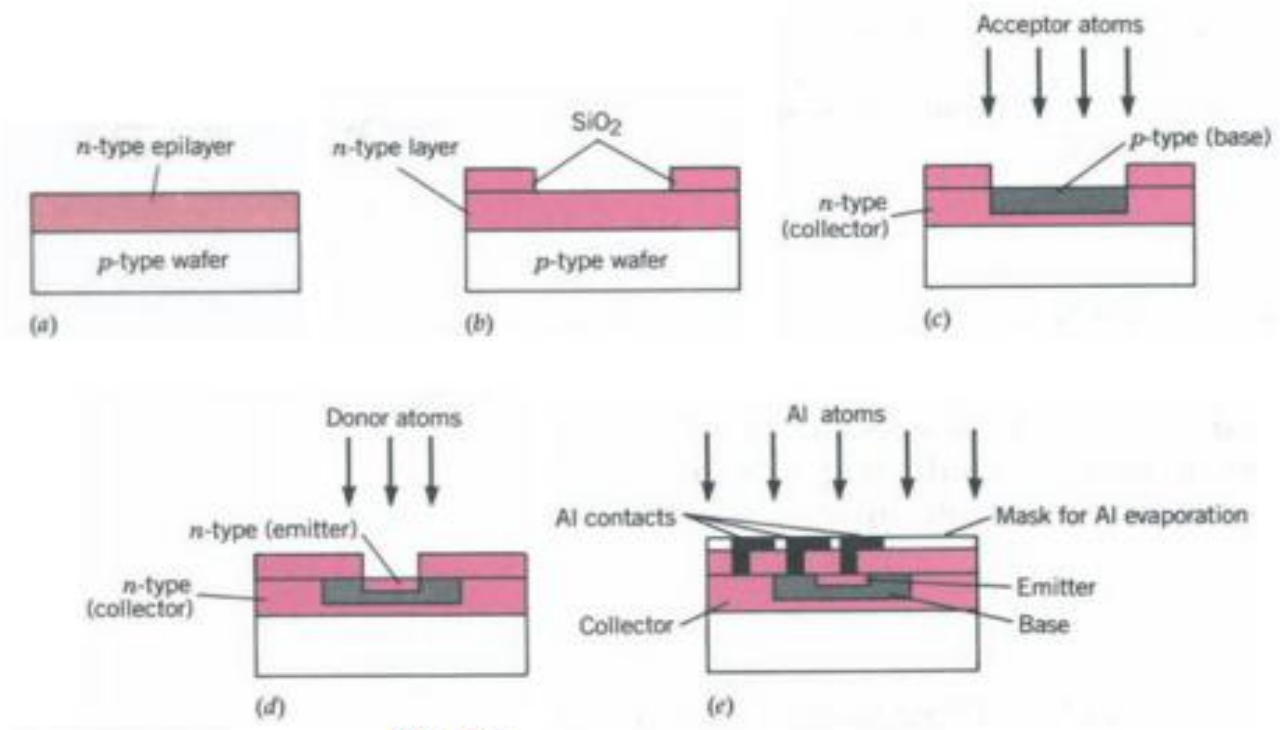


Figure:
Steps involved in the fabrication of a transistor on a silicon chip.

2. Resistors:

An integrated circuit resistor can be made by the shallow diffusion of a p-type channel into an n-type region or vice versa. The current is forced to flow through the channel by maintaining the channel at a negative voltage with respect to the surrounding n-type region. The resistance of the channel will be determined by its length, its cross section, as well as the doping concentration. Because of its relatively high conductivity, Si is not a useful material for a resistor. As a result, it is difficult to obtain large resistance values in ICs without using too much space in the chip. In cases where large resistors are needed, one standard approach is direct substitution. As we saw in Chapter 26, a transistor used in the common emitter configuration can be considered as a base current-controlled resistor. Thus, a transistor can be introduced in a circuit where a resistor is needed. The effective resistance between the collector and the emitter will be determined by the base current. Circuit designers often introduce transistors in a circuit where resistors might have been employed to save space on the chip.

3. Capacitors:

A capacitor is essentially two conducting electrodes separated by a very thin insulator. The first electrode of the microelectronic capacitor is usually made by doping very heavily (thus making it highly conductive) a region of the epitaxial layer. This region is covered with a Si02 layer as the insulator and the second

electrode is formed by evaporating a conducting aluminum film on the oxide layer. A schematic of an integrated circuit capacitor is shown in Fig.

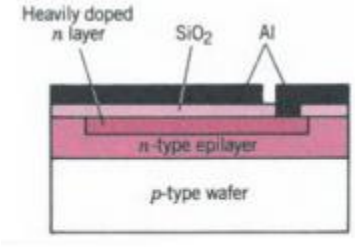


Figure: Microelectronic capacitor on a silicon chip.

4. Fabrication of a Simple IC (Fabrication of DTL NOR gate):

As we mentioned earlier, in the fabrication of an IC parts of several circuit components are often formed simultaneously. We will show how the simple NOR gate of Fig. can be made. The first step consists in growing three n-type islands on a p-type substrate. One of these islands will serve to construct the transistor, another the diodes, and the third the three resistors. These three islands are isolated electrically from one another by maintaining them at a positive potential with respect to the p-type substrate; that is, the substrate-islands junctions are reverse biased. To form these three islands, an n-type epilayer is grown onto the p substrate (Fig. a). The epilayer is then oxidized and coated with photoresist (Fig. b). The wafer is exposed to UV radiation through the mask shown in Fig. c. After developing the photoresist (removing the unexposed parts) and etching the wafer with HF (removing the unprotected Si02), the wafer has the form that is illustrated schematically in Fig.d. The exposed photoresist is dissolved away, and acceptor type impurities are diffused into the n-type epilayer. The diffusion is allowed to continue until the entire epilayer is converted to p-type, except for the three regions protected by the Si02 coating. A top view of the wafer at this stage is shown in Fig. e. The wafer is now reoxidized. Using the mask shown in Fig. f and following the procedure outlined earlier for window opening in the oxide layer (photoresist coating, masking, UV radiation, and so on), windows with the shape of the shaded areas of mask (f) are opened in the n-type islands. Acceptor-type impurities are diffused through these windows into the three n-type islands. In this case, the p-type dopant is not allowed to penetrate all the way through the n-type layers. When this step is completed, there are three resistors in the upper island, the collector and the base of an npn transistor in the lower left island, and two diodes with their n side common in the lower right island. The state of the chip is shown in Fig.g. The wafer is oxidized again, and, using the mask shown in Fig. h, a window is opened onto the base of the transistor for the diffusion of n-type dopants to form the emitter. All the circuit components are now in place, and they must now be interconnected. To achieve this, the wafer is reoxidized again, and, with the mask shown in Fig. i, small openings are made in the ends of the resistors, the three elements of the transistors, and both sides of the diodes. The wafer is then covered with the mask of Fig. j, and an aluminum evaporation is performed. The final structure is shown in Fig. k. The circuit is redrawn, using electronic symbols, in Fig.1.

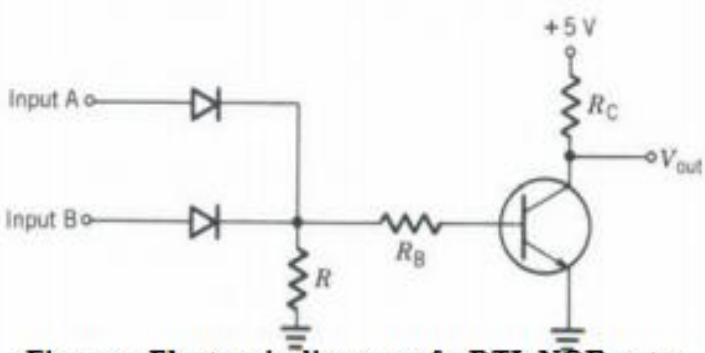
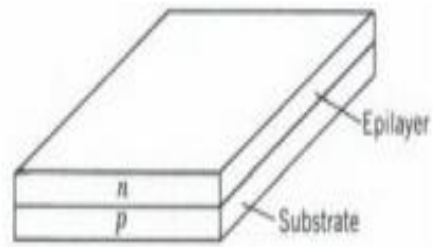
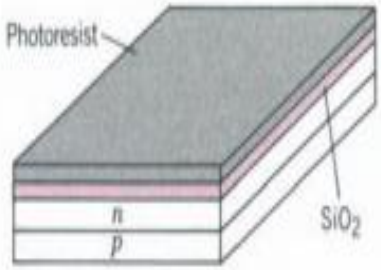


Figure a:Electronic diagram of a DTL NOR gate

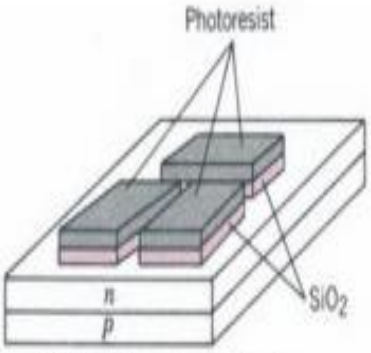


(a) *n*-type epitaxial layer grown on *p*-type wafer

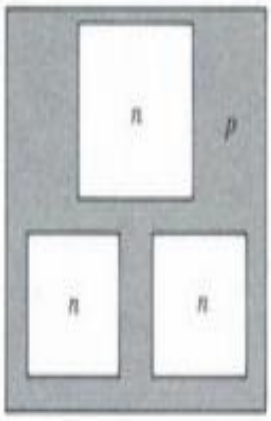


(b) Oxidation of *n*-type layer followed by photoresist coating

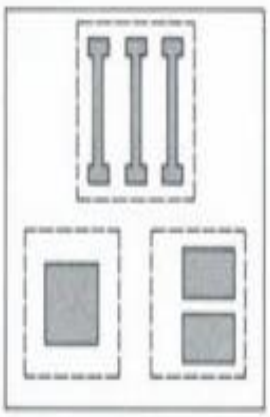
(c) Mask for *n*-type island formation



(d) Formation of oxide island with exposed photoresist on top

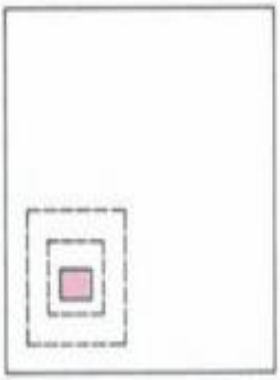


(e) Top view of wafer after *n*-type island formation

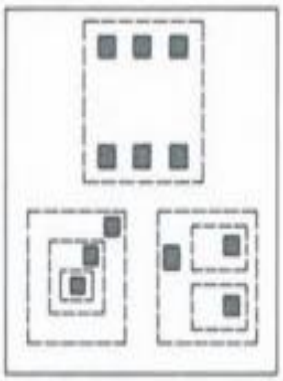


(f) Mask for *p* dopant diffusion

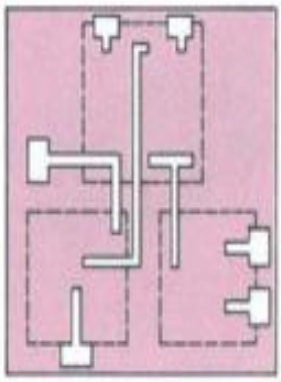
(*g*) State of the chip after *p*-type diffusion; shaded areas are *p*-type, white areas are *n*-type



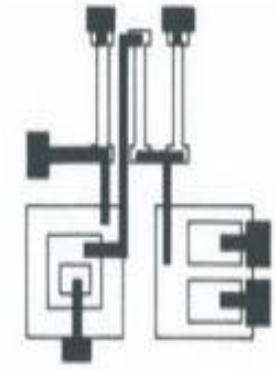
(*h*) Mask for emitter diffusion



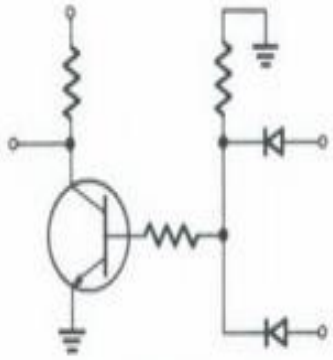
(*i*) Mask for electrical contact window-opening



(*j*) Mask for aluminum evaporation



(*k*) Complete and interconnected circuit



(*l*) Gate using conventional electronic symbols

Figure b: Steps involved in the fabrication of the NOR gate of fig a in integrated form.